**EENG 5550**

**Hardware Design Methodologies for ASICs and FPGAs**

**Spring 2023**

**Assignment 1**

**Assigned: January 26, 2023**

**Due: February 2, 2023**

In this assignment, you will design and synthesize the following designs using Xilinx Vivado:

1. 32:1 multiplexer using four 8:1 and one 4:1 multiplexer
2. 5-to-32 decoder
3. A 4-bit wide computational unit according to the following function table:

|  |  |  |
| --- | --- | --- |
| Selector | Operation | Function |
| “00” | Output <= Input | No shift |
| “01” | Output <= Shift-left (Input) | Shift Left |
| “10” | Output <= Shift-right (Input) | Shift Right |
| “11” | Output <= 0 | Zero output |

For each question above, submit vhdl code, RTL schematic, synthesis report, screenshots of simulation waveforms, and test bench of the designs. Test your design using at least five test cases. Mark two of the test cases and show the corresponding inputs, expected outputs and simulated outputs for those two cases. The source files should contain appropriate comments for better understanding.